AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1 to 15 (Cancelled)

16. (New) A semiconductor memory apparatus having a first axis and second axis orthogonal to the first axis, the apparatus comprising:

a connector comprising:

contacts arranged in a matrix; the contacts comprising:

a first set of contacts;

a second set of contacts; and

an allocation contact for receiving an external allocation signal; and

an integrated semiconductor memory comprising:

internal connections comprising a first set of connections and a second set of connections;

a signal generation device configured to generate an internal allocation signal having at least two states based on the external allocation signal received from the allocation contact; and

an allocation device connecting to the allocation contact and connecting the second set of connections with the second set of contacts, the allocation device is configured to allocate connections between the second set of connections and the second set of contacts based on the internal allocation signal received from the signal generation device.

17. (New) The apparatus of claim 16, wherein the integrated semiconductor memory further comprises external connections, each of the first set of connections connecting to a corresponding one of the external connections, each of the second set of connections configured to connect to a corresponding one of the external connections through the allocation device.

18. (New) The apparatus of claim 17, wherein the external connections are arranged in at least one row, the connections are positioned substantially in a center of the integrated semiconductor memory.

19. (New) The apparatus of claim 16, wherein the second set of connections comprises address connections.

20. (New) The apparatus of claim 16, wherein the second set of connections comprises command connections.

21. (New) The apparatus of claim 16, wherein the at least two states comprise a first state and a second state; wherein when the internal allocation signal is in the first state, connections of the second set of contacts are in a first connection arrangement; and

wherein when the internal allocation signal is in the second state, connections of the second set of contacts are symmetrical to the first connection arrangement about the first axis.

22. (New) The apparatus of claim 21, wherein the at least two states comprise a first state and a second state; and

wherein when the internal allocation signal is in the second state, connections of the second set of contacts are symmetrical to the first connection arrangement about the second axis.

23. (New) The apparatus of claim 22, wherein the at least two states comprise a third state; and

wherein when the internal allocation signal is in the third state, connections of the second set of contacts are symmetrical to the first connection arrangement about the second axis.

24. (New) The apparatus of claim 22, wherein the at least two states comprise a third state;

wherein when the internal allocation signal is in the third state, connections of the second set of contacts are symmetrical to the first connection arrangement about the first axis.

25. (New) The apparatus of claim 23, wherein the at least two states comprise a fourth state; and

wherein when the internal allocation signal is in the fourth state, connections of the second set of contacts are symmetrical to the first connection arrangement about the first axis and the second axis.

26. (New) The apparatus of claim 24, wherein the at least two states comprise a fourth state; and

wherein when the internal allocation signal is in the fourth state, connections of the second set of contacts are symmetrical to the first connection arrangement about the first axis and the second axis.

27. (New) The apparatus of claim 16, wherein the contacts comprise a ball grid array.

28. (New) The apparatus of claim 16, wherein the allocation device comprises logic gates.

29. (New) The apparatus of claim 16, wherein the second set of contacts are arranged symmetrically with respect to the first axis.

30. (New) The apparatus of claim 16, wherein the second set of contacts are arranged symmetrically with respect to the second axis.

31. (New) The apparatus of claim 16, wherein the signals that are transmitted between the internal connections and the contacts remain substantially unchanged during transmission.

32. (New) A semiconductor memory apparatus system, comprising:

a first semiconductor apparatus and a second semiconductor apparatus, each semiconductor apparatus comprising:

a connector comprising:

contacts arranged in a matrix; the contacts comprising:

a first set of contacts;

a second set of contacts; and

an allocation contact for receiving an external allocation signal; and

an integrated semiconductor memory comprising:

internal connections comprising a first set of connections and a second set of connections;

a signal generation device configured to generate an internal allocation signal having at least two states based on the external allocation signal received from the allocation contact; and

an allocation device connecting to the allocation contact and connecting the second set of connections with the second set of contacts, the allocation device is configured to allocate connections between the second set of connections and the second set of contacts based on the internal allocation signal received from the signal generation device; and

a printed circuit board having a first side and a second side opposite the first side; the board comprising at least one allocation supply connection configured to be connected to an allocation contact;

wherein the first semiconductor memory apparatus is positioned on the first side and the second semiconductor apparatus is positioned on the second side opposite the first semiconductor memory apparatus.

33. (New) The system of claim 32, wherein the at least two states comprise a first state and a second state;

wherein during operation, the allocation contact of the first semiconductor memory apparatus is not connected to the printed circuit board and the internal allocation signal of the first semiconductor memory apparatus is in the first state; and

wherein the allocation contact of the second semiconductor memory apparatus is connected to one of the at least one allocation supply connections of the printed circuit device and the internal allocation signal of the second memory apparatus is in the second state.

34. (New) The system of claim 33, wherein the at least two states comprise a third state; and

wherein the at least one allocation supply connections are configured to connect to the allocation contact of one of the semiconductor memory apparatuses, the internal allocation signal of the second semiconductor apparatus is in a second state or a third state based on the allocation supply connection connected to the allocation contact of the second semiconductor supply connection.

35. (New) The system of claim 32, wherein the at least two states comprise a first state, a second state, a third state and a fourth state, wherein the printed circuit board comprises at least four allocation supply connections, each allocation supply contact is connected to a corresponding allocation supply connection, the internal allocation signal of the second semiconductor memory apparatus is in the second or third state and the internal allocation signal of the first semiconductor memory apparatus is in the first or fourth state based on the connection

between the allocation supply connection and the allocation contact of the second semiconductor memory.